UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/669,034	09/25/2000	Ganesh Subramaniyam	042390.P9043	3498

7590 03/23/2004

Mark L Watson
Blakely Sokoloff Taylor & Zafman LLP
Seventh Floor
12400 Wilshire Boulevard
Los Angeles, CA 90025-1026

EXAMINER	
PHAN, RAYMOND NGAN	
ART UNIT	**PAPER NUMBER**
2111	13

DATE MAILED: 03/23/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

UNITED STATES PATENT AND TRADEMARK OFFICE

Commissioner for Patents
United States Patent and Trademark Office
P.O. Box 1450
Alexandria, VA 22313-1450
www.uspto.gov

BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Paper No. 13

Application Number: 09/669,034
Filing Date: September 25, 2000
Appellant(s): Subramaniyam et al.

Mark L. Watson
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed on Jan 12, 2004, paper No. 12. Remaining at issue is the rejection under 35USC103 of claims 1-24.

1. The statement of the status of claims contained in the brief is correct.
2. The appeal involves claims 1-24, in the case.
3. No claims have been allowed.
4. No claims have been objected.
5. The appellant's statement of the status of amendment after final rejection contained in the brief is correct.

The text of those actions of Title 35 U.S.C. Code relied upon in this appeal can be found as presented below.

The following is a listing of the prior art of record relied upon in the rejection of claims under appeal.

Hetherington et al. (US No. 5,978,864)	November 2, 1999
Shiell et al. (US No. 6,138,232)	October 24, 2000
McFarland et al. (US No. 5,125,093)	June 23, 1992

I. The summary of invention contained in the brief on pages 4-5 is correct.

II. The copy of the appealed claims 1-24 contained in the Appendix to the brief is correct.

III. The appellant's brief includes a statement that the rejection of claims 1-24 stand or fall together and provides reasons as set forth in 37C.F.R.1.192(c)(5) and (c)(6).

IV. The appellant's statement of the issues in the brief on page 6 is correct.

V. No new prior art has been applied in this examiner's answer.

***Grounds of Claim Rejections - 35 USC §103 (claims* 1-24)**

6. Claims 1-3, 8, 8-24, are rejected under 35 U.S.C. § 103(a) as being unpatentable over Hetherington et al. (US No. 5,978,864) in view of Shiell et al. (US NO. 6,138,232).

In regard to claims 1, 8, Hetherington et al. disclose a method and system comprising a CPU 200, wherein the CPU includes power management logic 220 that enables the CPU to operate in a first execution mode (reduced at step 506) whenever the temperature of the CPU exceeds the predetermined threshold

(threshold at step 502) (see col. 13, lines 44-55) and operates in a second execution mode (normal at step 510) whenever the temperature of the CPU is below the predetermined threshold (threshold at step 508) (see figures 2 and 5, col. 14, lines 5-32). But Hetherington et al. do not specifically disclose the first quantity of instruction per cycle in first mode and second quantity of instructions per cycle in second mode. However Shiell et al. disclose the first quantity of instruction per cycle in first mode (i.e. partial mode) (see col. 9, lines 16-20) and second quantity of instructions per cycle in second mode (i.e. full mode) (see col. 9, lines 25-40). Therefore, it would have been obvious to a person of an ordinary skill in the art at the time the invention was made to have combined the teachings of Shiell et al. within the system of Hetherington et al. because it would reduce the power consumption in the computer system (see col. 9, lines 47-52).

In regard to claims 2, 15, Hetherington et al. disclose wherein the power management logic comprising a thermal sensor 220 (see col. 13, lines 44-54); and an interrupt generating hardware coupled to the digital filter, wherein the interrupt generating hardware generates a first interrupt whenever the temperature of the CPU exceeds the predetermined threshold (see step 504) and generates a second interrupt whenever the temperature of the CPU is below the predetermined threshold (see step 510) (see col. 14, lines 5-32). The teaching of digital filter is inherently known to the teaching of Hetherington et al. because the step of determining 502 if the temperature exceeded or crossed a predetermined programmed threshold level which is the digital filter of the teaching of Hetherington et al. (see Shiell, col. 13, lines 44-55).

In regard to claims 3, 24, Hetherington et al. disclose the step of determining the temperature exceeds or crossed a predetermined programmed threshold level

(i.e. digital filter) (see col. 13, lines 46-55). The teaching of an analog to digital converter coupled between the thermal sensor is inherently known to the teaching of Hetherington et al. because the thermal sensing circuit 220 of Hetherington receive the temperature signal which must be an analog signal and determined the temperature to the programmed threshold level (a digital signal) in order to output the NMI signal thereby there must be an A/D mechanism to convert the analog signal (a temperature signal) to a digital signal to compare to the programmed threshold level (see col. 13, lines 46-55).

In regard to claims 9, 17, 21, Hetherington et al. disclose wherein the power management logic further comprises an instruction execution unit coupled to the interrupt handler (step 504) (see figure 5); and an artificial activity generator coupled to the interrupt handler (see col. 14, lines 32-67). Hetherington et al. disclose the queue activity rise time detector which generates the stall signal (step 606) wherein the ISU 206 and IRU 204 is the queue activity source (see col. 14, lines 30-47).

In regard to claims 10, 19, 23, Hetherington et al. disclose wherein the artificial activity generator causes the CPU artificial activity generator to suspend artificial activity within the CPU whenever the die temperature is above the predetermined threshold temperature (see col. 14, lines 5-22). Hetherington et al. disclose the queue activity rise time detector which generates the stall signal (step 606) wherein the ISU 206 and IRU 204 is the queue activity source (see col. 14, lines 30-47).

In regard to claims 11-14, 18, 22, Hetherington et al. disclose wherein the instruction execution unit causes the CPU to operate in a full dispersal mode (step 510) whenever the die temperature is below the predetermined threshold

temperature (step 508) and operates in a single dispersal mode (step 506) whenever the temperature of the CPU is above the predetermined threshold temperature (step 502) (see figure 5, col. 14, lines 47-67).

In regard to claims 16, 20, Hetherington et al. disclose wherein the power management logic comprising a thermal sensor 220 (see col. 13, lines 44-54); and an interrupt generating hardware coupled to the digital filter, wherein the interrupt generating hardware generates a first interrupt (step 504) whenever the temperature of the CPU exceeds the predetermined threshold (step 502) (see figure 5) and generates a second interrupt (step 510) whenever the temperature of the CPU is below the predetermined threshold (step 508) (see figure 5, col. 14, lines 5-32). The teaching of digital filter is inherently known to the teaching of Hetherington et al. Hetherington et al. disclose the step of determining the temperature exceeds or crossed a predetermined programmed threshold level (i.e. digital filter) (see col. 13, lines 46-55). The teaching of an analog to digital converter coupled between the thermal sensor is inherently known to the teaching of Hetherington et al. because the thermal sensing circuit 220 of Hetherington receive the temperature signal which must be an analog signal and determined the temperature to the programmed threshold level (a digital signal) in order to output the NMI signal thereby there must be an A/D mechanism to convert the analog signal (a temperature signal) to a digital signal to compare to the programmed threshold level (see col. 13, lines 46-55).

7. Claims 4-7 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Hetherington et al. in view of Shiell et al. and further in view of McFarland et al. (US No. 5,125,093)

In regard to claim 4, Hetherington et al. and Shiell et al. teach the claimed subject matter as discussed above except the teaching of PAL wherein the PAL includes an interrupt handler for receiving the first and second interrupt. However McFarland et al. disclose the PAL wherein the PAL includes an interrupt handler for receiving interrupts (see col. 8, lines 38-56). Therefore, it would have been obvious to a person of an ordinary skill in the art at the time the invention was made to have combined the teachings of McFarland et al. within the system of Hetherington et al. and Shiell et al. because it would provide a technique that efficiently allocates the servicing of multiple interrupts.

In regard to claim 5, Hetherington et al. disclose wherein the power management logic further comprises an instruction execution unit coupled to the interrupt handler (step 504) (see figure 5); and an artificial activity generator coupled to the interrupt handler (see col. 14, lines 32-67). Hetherington et al. disclose the queue activity rise time detector which generates the stall signal (step 606) wherein the ISU 206 and IRU 204 is the queue activity source (see col. 14, lines 30-47).

In regard to claim 6, Hetherington et al. disclose wherein the instruction execution unit causes the CPU to operate in a full dispersal mode whenever the die temperature is below the predetermined threshold temperature and operates in a single dispersal mode whenever the temperature of the CPU is above the predetermined threshold temperature (see col. 13, line 37 through col. 14, line 30). Shiell et al. disclose one, two, and four instructions per cycle. Thus one skilled in

the art would naturally implement six instructions per cycle to the capability of Shiell processor and processing technique to increase the processing of instructions. Therefore, it would have been obvious to a person of an ordinary skill in the art at the time the invention was to expand the number of instructions per cycle beyond the capacity of Shiell processor to increase the capability of processing of the processor with power conservation.

In regard to claims 7, Hetherington et al. disclose wherein the artificial activity generator causes the CPU artificial activity generator to suspend artificial activity within the CPU whenever the die temperature is above the predetermined threshold temperature (see col. 14, lines 5-22). Hetherington et al. disclose the queue activity rise time detector which generates the stall signal (step 606) wherein the ISU 206 and IRU 204 is the queue activity source (see col. 14, lines 30-47).

Rebuttal

8. The Examiner has carefully considered the arguments set forth by appellant in the brief and finds the argument to be unpersuasive.

In the brief, appellant argued in substance as to the rejection of claims 1, 8, 16, and 20:

(1) neither Hetherington nor Shiell disclose or suggest a CPU to execute a first quantity of instruction per cycle when the temperature of the CPU exceeds a predetermined threshold and to execute a second quantity of instruction per cycle when the temperature of the CPU is below a predetermined threshold.

(2) Hetherington does not teach or suggest a combination with Shiell and that Shiell does not teach or suggest a combination with Hetherington.

(3) Appellant submits that it would be impermissible hindsight based Appellant's own disclosure to incorporate the Shiell interrupt service mechanism into Hetherington's thermal overload detection and prevention mechanism.

(4) McFarland does not disclose or suggest a CPU to execute a first quantity of instruction per cycle when the temperature of the CPU exceeds a predetermined threshold and to execute a second quantity of instruction per cycle when the temperature of the CPU is below a predetermined threshold.

As (1), Hetherington et al. disclose a power management logic that enables the CPU to operate in a first execution mode (reduced step 506) whenever the temperature of the CPU exceeds the predetermined threshold (step 502) (see col. 13, lines 37-55) and to operate in a second execution mode (normal step 510) whenever the temperature of the CPU is below the predetermined threshold (step 508) (see figure 5, col. 13, lines 54 through col. 14, line 4). Hetherington et al. disclose the sensing circuit 220 which monitors the temperature of the processor 200 if the temperature exceeds or crossed a predetermined programmable threshold level (i.e. digital filer), a non-maskable interrupt is issued to the processor to reduce the frequency (see figure 5, col. 13, lines 44-55). But Hetherington et al. do not specifically disclose the first quantity of instruction per cycle in first mode and second quantity of instructions per cycle in second mode. However Shiell et al. disclose the first quantity of instruction per cycle (i.e. single instruction per cycle) in first mode (i.e. partial speculative mode) (see table 1, col. 9, lines 19-25) and second quantity of instructions per cycle (i.e. 4 instructions per cycle) in second mode (i.e. full speculative mode) (see table 1, col. 9, lines 31-40). Shiell et al.

disclose one, two, and four instructions per cycle. Thus one skilled in the art would naturally implement six or eight instructions per cycle to the capability of Shiell processor and processing technique to increase the processing of instructions. Therefore, it would have been obvious to a person of an ordinary skill in the art at the time the invention was to expand the number of instructions per cycle beyond the capacity of Shiell processor to increase the capability of processing of the processor with power conservation.

As (2), Hetherington suggests the queue activity rise time detector 306 continuously monitoring instruction queue activity from the queue activity source in order to reduce the rate of the processor (see col. 14, lines 22-47). Both Hetherington and Shield mentioned by reducing the rate of the processor, thus reducing the power consumption (see Shiell, col. 9, lines 47-55). In response to applicant's argument that there is no suggestion to combine the references, the examiner recognizes that obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. See *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988)and *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992). In this case, the combination of Hetherington and Shiell.

As (3), In response to applicant's argument that the examiner's conclusion of obviousness is based upon improper hindsight reasoning, it must be recognized that any judgment on obviousness is in a sense necessarily a reconstruction based upon hindsight reasoning. But so long as it takes into account only knowledge which was within the level of ordinary skill at the time the claimed invention was

made, and does not include knowledge gleaned only from the applicant's disclosure, such a reconstruction is proper. See *In re McLaughlin*, 443 F.2d 1392, 170 USPQ 209 (CCPA 1971).

As (4), in response to applicant's arguments against the references individually, one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.*, 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986).

VI. For the reasons started hereinabove, the Examiner believes that the rejections should be sustained.

Respectfully submitted,

PAUL R. MYERS
PRIMARY EXAMINER

Raymond Phan
March 16, 2004

Appeal Brief Conferees:

TOD SWANN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100